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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,515	10/26/2001	Chien-Hsin Lin	US018145	3418

7590 09/14/2004

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EXAMINER	
ROSARIO-VASQUEZ, DENNIS	
ART UNIT	**PAPER NUMBER**
2621	4

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,515	LIN ET AL.	
	Examiner	Art Unit	
	Dennis Rosario-Vasquez	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Receipt of the PCT search report received on April 24, 2003 has been acknowledged

Specification

2. The disclosure is objected to because of the following informalities:

Page 7, line 22 has the phrase "filter 210 follows filter 220" which ought to be amended to "filter 210 **comes after** filter 220". The phrase corresponds with figure 2B, which shows filter 220 processed first and filter 210 second.

Page 10, line 7: "buffers" ought to be amended to "buffer".

Page 10, line 11:"8-tap, 64-phase" ought to be amended to "8-tap, 64-phase".

Appropriate correction is required.

Claim Objections

3. The following quotations of 37 CFR § 1.75(a) is the basis of objection:

> (a) The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

4. Claims 1 and 10 are objected to under 37 CFR § 1.75(a) as failing to particularly point out and distinctly claim the subject matter which the applicant regards as his invention or discovery.

Claim 1, lines 8,9 has the phrase "the first operational mode" which ought to be amended to "a first operational mode".

Claim 10, lines 9,10 has the phrase "the first operational mode" which ought to be amended to "a first operational mode".

In addition, claims 1, lines 8-13 states," a logic circuit adapted to cause the vertical processing circuit to operate in **the** (emphasis added) first operational mode in which the filtered data is processed by using the first set of coefficients and circulating **the filtered data** (emphasis added) through the line-buffer circuit and to switch between the first operational mode and a second operational mode in which the vertical processing circuit performs another function by using a set of coefficients that is different than the first set of coefficients. "

In claim 1, line 10, the phrase "the filtered data" does not correspond with the specification. Claim 1, line 10 is interpreted as data that was filtered is inputted back to the line buffer. No support in the specification was found for this interpreted feature.

Claim 10, line 10 has the phrase "the filtered data" which has the same problem of claim 1, line 10.

Pages 10-11 correspond with claim 1 in which data is accessed from a buffer to be filtered, and no mentioning of "the filtered data" is returned to the buffer.

Claim 1, line 10 has the phrase "the filtered data" which ought to be amended to "the pixel data" which refers to line 3 of "pixel data".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Niehaus (US Patent 5,422,827 A).

Regarding claims 1 and 10, Niehaus discloses a pixel-data processing arrangement and method, comprising:

a) a vertical processing means (fig. 1. numerals 101 and 103) including a polyphase filter means (Fig. 1, num. 103) and a line-buffer circuit means (fig. 1, num. 101), the vertical processing means (fig. 1, numerals 101 and 103) adapted to receive (fig. 1, num. 101 has an input arrow.) and circulate pixel data (fig. 1, num. 102) and through the line-buffer circuit means (fig. 1, num. 101) and from the line-buffer circuit means (output of fig. 1, num. 101) to the polyphase filter means (fig. 1, num. 103), the polypahse filter means (fig. 1 ,num. 103) being adapted to filter the pixel data (The output of fig. 1, num. 103 is filtered data of fig. 1, num. 102.) and perform peaking (Fig. 1, num. 108:"SHARPNESS") and scaling functions (Fig. 1, num. 107) concurrently ("single step" as mentioned in col. 3, lines 38-42.) by using a first set of coefficients (Fig. 6, num. 607 is a coefficient graph as mentioned in col. 9, lines 64 and 65 with the coefficients (-0.2-1.00) on the vertical axis that correspond with graph 607. Note that fig. 5 and fig. 6 are coefficient graphs.), the first set of coefficients (Fig. 6, num. 607 is a

coefficient graph as mentioned in col. 9, lines 64 and 65.) resulting from a convolution (The functions of Fig. 3a and 3b are combined into a function shown in fig. 3c and mentioned in col.9, lines 5-16.) of peaking filter coefficients (Fig. 6 has a sharpening factor that considers "peaks" of 1.00 or 0.80 or 0.68 as mentioned in col. 11, lines 11-16 and 28-36.) with scaling filter coefficients (Fig. 6, label "X_SCALE=1.5" that corresponds with each peaking filter coefficient as mentioned in col. 11, lines 8,9.); and

b) a logic circuit (fig. 1, num. 108) adapted to cause the vertical processing circuit means (fig. 1, numerals 101 and 103) to operate in **the** first operational mode (Scaling or "X_SCALE" using a factor of 1.5 and sharpening or "sh" using a factor of 0.80 is shown in figure 6.) in which the filtered data (The output of fig. 1, num. 103 is filtered data of fig. 1, num. 102.) is processed by using the first set of coefficients (Fig. 6, num. 607 is a coefficient graph as mentioned in col. 9, lines 64 and 65.) and circulating **the filtered data** (The output of fig. 1, num. 103 is filtered data of fig. 1, num. 102 or fig. 1, num. 102 pending upon the above claim objections.) through the line-buffer circuit means (fig. 1, num. 101) and to switch between the first operational mode (Fig. 6, num 606) and a second operational mode (Fig. 6, num. 607) in which the vertical processing circuit means (fig. 1. numerals 101 and 103) performs another function (Fig. 6, num. 605) by using a set of coefficients (Fig. 6 has a vertical axis of coefficients.) that is different (The graph of 605 corresponds to a set of coefficients on the vertical axis that is different from the graph of 607.) than the first set of coefficients (Fig. 6, num. 607 is a coefficient graph as mentioned in col. 9, lines 64 and 65.).

Regarding claim 2, Niehaus discloses the pixel-data processing arrangement of claim 1, further including a storage unit (Fig. 1, num. 109:MEMORY) adapted to receive and store processed pixel data (MEMORY 109 receives processed data from 105:DECIMATOR), and wherein the first operational mode (Scaling or "X_SCALE" using a factor of 1.5 and sharpening or "sh" using a factor of 0.80 is shown in figure 6.) the vertical processing circuit (fig. 1. numerals 101 and 103) receives the pixel data (fig. 1, num. 102) at a first rate("input rate" as mentioned in col. 5, line 54.) and outputs the processed pixel data (from DECIMATOR 105 of fig. 1) for storage in the storage unit (Fig. 1, num. 109:MEMORY) at a second pixel rate ("output rate that is half of the input rate" as mentioned in col. 5, lines 53,54), the second pixel ("output rate that is half of the input rate" as mentioned in col. 5, lines 53,54) rate being different (Both rates are at different rates.) than the first pixel rate ("input rate" as mentioned in col. 5, line 54.).

Regarding claim 3, Niehaus discloses the pixel-data processing arrangement of claim 2, wherein the first pixel rate ("input rate" as mentioned in col. 5, line 54.) is faster (by half) than the second pixel rate ("output rate that is half of the input rate" as mentioned in col. 5, lines 53,54).

Claim 4 has different claim language than claim 3, but both claims are performing the same function therefore claim 4 has been addressed in claim 3.

Regarding claim 5, Niehaus discloses the pixel-data processing arrangement of claim 1, wherein the other function (Fig. 6, num. 605) performed by the vertical processing circuit (fig. 1. numerals 101 and 103) is an N-taps scaling function (Interpolating filters with different numbers of taps as mentioned in col. 6, lines 43-45.), where N is an integer greater than 2 (One filter has three times as many the number of taps as another filter as mentioned in col. 6, lines 64-66.).

Regarding claim 6, Niehaus discloses the pixel-data processing arrangement of claim 1, wherein the other function (Fig. 6, num. 605) performed by the vertical processing circuit (fig. 1. numerals 101 and 103) is an N-taps averaging-filter function ("weighted average" is outputted from 103 of fig. 1 and performed in step 206:"APPLY COEFFICIENTS TO SAMPLE AND NEIGHBORS" of fig. 2.) in which pixel neighboring ("NEIGHBORS" of step 206.) a current pixel ("SAMPLE" in step 206 of fig. 2) are averaged ("weighted average" is outputted from 103 of fig. 1) and where N is an integer greater than 2 (Addressed in claim 5.).

Regarding claim 7, Niehaus discloses the pixel-data processing arrangement of claim 1, wherein the first set of coefficients (Fig. 6, num. 607 is a coefficient graph as mentioned in col. 9, lines 64 and 65.) results from a convolution(The equation in col. 9, line 15 is a combination of two filters as mentioned in col. 9, lines 6-16.) of 3 taps (Filter 1 has an integer multiple of the number of taps as filter 2 as mentioned in col. 6, lines 63-65. Therefore filter 1 has 8 taps.) of the peaking filter coefficients (Fig. 6 has a sharpening factor that considers "peaks" of 1.00 or 0.80 or 0.68 as mentioned in col. 11, lines 11-16 and 28-36.) with 4 taps (While filter 2 has 4 taps.) of scaling filter coefficients (Fig. 6, label "X_SCALE=1.5" is shown three times).

Regarding claims 8 and 9, Niehaus discloses the pixel-data processing arrangement of claim 1, wherein the vertical processing circuit (fig. 1. numerals 101 and 103) and logic circuit (fig. 1, num. 108) are implemented using a programmed processor ("programmable processor" as mentioned in col. 1, line 66. The programmable processor changes filter parameters. Note that fig. 1, num. 106 is a logic circuit that controls the filter parameters. Thus, fig. 1, num. 106 is also implemented with the programmable processor.).

Claim 11 has been addressed in claim 1.

Claim 12 has been addressed in claim 5.

Claim 13 has different functional language than claims 6 and 7, but claim 13 has the functions of claims 6 and 7. Thus, claim 13 has been addressed in claims 6 and 7.

Regarding claim 14, Niehaus discloses a pixel-data processing arrangement, comprising:

a) storage means(fig.1, num. 109) for receiving and storing pixel data;

b) processing means ("programmable processor" as mentioned in col. 1, line 66.) for processing pixel data (fig. 1, num. 102), the processing means ("programmable processor" as mentioned in col. 1, line 66.) including a vertical processing means (fig. 1, num. 101 and 103) including a polyphase filter (fig. 1, num. 103) and a line-buffer circuit (fig. 1, num. 101), the vertical processing means (fig. 1, num. 101 and 103) having a first operational mode (fig. 3a is a filter response.) in which pixel data (fig. 1, num. 102) is received at a first pixel rate ("input rate" in col. 5, line 54.) and circulated through the line-buffer circuit (fig. 1, num. 101), the circulated data (The output of fig. 1, num. 101 is circulated data.) being manipulated by the vertical processing means (Fig. 1, num. 101 and 103.), and the vertical processing means (fig. 1, num. 101 and 103) being configured to perform a first function ("F1" is a frequency response as mentioned in col. 9, lines 18,19.) using a first set of operating coefficients ("c" in col. 9, lines 20,21), and the processed pixel data (The output of fig. 1, num. 101 is processed pixel data.) is output for storage (via num. 105) in the storage means (fig. 1, num. 109) at a second pixel rate ("output rate" in col. 5, line 53), the second pixel rate ("output rate" in col. 5, line 53) being different (The output rate is half the input rate as mentioned in col. 5, lines 53,54) than the first pixel rate ("input rate" in col. 5, line 54.); and

c) means (fig. 2 is a program) for causing the processing means ("programmable processor" as mentioned in col. 1, line 66.) to switch between the first operational mode (fig. 3a is a filter response.) and one of at least two other selectable operational modes (fig. 3b and 3c are filter responses.), each of the at least two other selectable operational (fig. 2, num. 202 allows for selecting curves or filter responses.) modes including circulating data (Fig. 3b and 3c are filter responses for pixel data.) for processing by the vertical processing means (fig. 1, num. 101 and 103.), wherein the first set of operating coefficients ("c" in col. 9, lines 20,21) are pre-determined ("c" has a range from 0.6 to 1.0 as mentioned in col. 9, lines 20,21.) from a convolution of a second set of operating coefficients (The equation in col. 9, line 16 has a second set of operating coefficients on the right hand side of the minus sign.) defining a second data-manipulation function ("F2" is another filter response as mentioned in col. 9, line 19,20.) and a third set of operating coefficients (All the "c" values from the equation in col. 9, line 16.) defining a third data-manipulation function ("G" is a filter response as mentioned in col. 9, line 18.), and the first function ("F1" is a frequency response as mentioned in col. 9, lines 18,19.) providing a result that is the same as a result that would be provided by the second and third functions being performed cascaded (Niehaus states,"The current state of the art involves scaling the image...and then scaling down. This requires two different sets of filters [F1 and F1 above] to perform one operation [G above]. The present invention merges these two operations [F1 and F2] into one filter [G]...(col. 6, lines 16-20).

Claim 15 has been addressed in claim 3.

Claim 16 has been addressed in claim 4.

Claim 17 has been addressed in claim 5.

Claim 18 has been addressed in claim 13.

Claim 19 has been addressed in claim 7.

Claims 20 and 21 have been addressed in claim 8.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stessen et al. (US patent 6,700,626 B2) is pertinent as teaching a method of cascading peaking filters as mentioned in the abstract.

Shen et al. (WO 01/45389 A1) is pertinent as teaching a method of using a peaking filter (fig. 1, num. 190) with a buffer (fig. 1, num. 150) and coefficients (fig. 1, num. 181).

Bolger (US Patent 4,538,178 A) is pertinent as teaching a method of using a filter (fig. 1, num. 12) with a peaking controller (fig. 1, num. 40) and coefficient generation (fig. 1, num. 30).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario-Vasquez whose telephone number is 703-305-5431. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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